

1 FABRICATION OF SEMICONDUCTOR DIES WITH MICRO-PINS
2 AND STRUCTURES PRODUCED THEREWITH

3
4 FIELD OF THE INVENTION
5

6 The present invention relates to the packaging and
7 assembly of integrated circuit. More particularly, it
8 relates to a method and apparatus for connecting
9 integrated circuits to one another and to other devices
10 so as to preserve space and so as to create compact
11 electronic packages.

12
13 BACKGROUND OF THE INVENTION
14

15 Integrated circuits (ICs) or chips are typically
16 connected to packages or directly on to a system board
17 by use of wire bonds or solder bumps that lie on the
18 surface of the ICs. To achieve a compact and higher
19 performance electronic system, it is desirable to stack
20 ICs (in bare or packaged form) on top of each other.
21 Such a stack of ICs may then be packaged using methods
22 that are conventionally used to package an IC and
23 connected to the next level of packaging.

24
25 ICs are typically stacked by use of wire bonds or
26 conductive thru-vias that are fabricated within the IC.
27 The art of stacking ICs using wire bonds has been
28 previously published in the literature. Examples are
29 Kiyono, S. S., Yamada, T., Yonehara K., "Consideration
30 of Chip Circuit Damage on DCS - FBGA Packages," 52nd
31 Electronic Components and Technology Conference, May
32 2002, San Diego, California. and Intel Stacked Chip

1 Scale Packaging Products, available at
2 <http://www.intel.com/design/flcomp/prodbref/298051.htm>.
3 In this approach, a smaller chip is attached on top of
4 a larger chip with the use of an adhesive. The smaller
5 chip is either wire-bonded to a portion of a larger
6 chip or directly wire-bonded to the package substrate.
7 Because a wire bond connection has to be made to all of
8 the chips in the stack, it is required that a chip in
9 the stack be smaller than a chip underneath it. As a
10 result, the size of the chips that can be stacked is
11 limited. To be able to stack chips of the same size, a
12 spacer of specific height and dimension can be inserted
13 between the chips. Wu, L., Wang, Y. P., Hsiao C. S.,
14 "Innovative Stack-Die Package - S2BGA," 52nd Electronic
15 Components and Technology Conference, May 2002, San
16 Diego, California. Such spacer will separate the chips
17 and will allow enough working distance to enable a wire
18 bond connection. However, the addition of a spacer
19 increases the height of the stack and also adds extra
20 process steps that may complicate and deteriorate the
21 assembly and reliability of the stack. Further, when a
22 spacer is used, it is difficult to make an electrical
23 connection between chips in the stack.
24
25 To overcome the limitations of wire bond IC stacks, an
26 alternate approach involving use of conductive
27 thru-vias fabricated within the IC has also been
28 introduced, by Sunohara, M., Fujii, T., Hoshino, M.,
29 Yonemura H., Tomisaka, M., Takahashi, K., "Development
30 of Wafer Thinning and Double-Sided Bumping Technologies

1 for the Three-dimensional Stacked LSI," 52nd Electronic
2 Components and Technology Conference, May 2002, San
3 Diego, California. In this approach, vias are
4 fabricated into the IC and filled with a conductor.
5 During subsequent process steps, electrical connections
6 are made to these thru-vias, the IC wafer is attached
7 to a carrier wafer, thinned down to expose the thru-via
8 conductor, insulated on the backside and attached to
9 another IC formed using similar process flow. A
10 significant number of expensive process steps are
11 applied to an active, and often thin, IC wafer in this
12 approach. Expensive IC area is used to fabricate
13 conductive thru-vias. In addition, the resultant
14 structure may have poor thermo-mechanical reliability
15 because of a large difference in the Coefficient of
16 Thermal Expansion (CTE) between silicon and the
17 conductive material that is used to fill a thru-via.
18 Assembly processes during IC stacking may introduce
19 mechanical stress that can lead to silicon fracture.

20

21 It would be desirable to have a structure and a
22 corresponding process flow that can be easily
23 integrated with semiconductor back end of the line
24 (BEOL) processes and as a result, provides an effective
25 way to either stack ICs on top of each other or
26 assemble them vertically adjacent to each other
27 achieving, in the end, a higher level of system
28 integration by utilising three dimensions.

29

30

1 SUMMARY OF THE INVENTION

2
3 It is therefore an aspect of the present invention to
4 provide a semiconductor with pins that facilitate
5 electrical connection.

6
7 It is another aspect of the invention to provide a
8 method of manufacturing such semiconductor dies.

9
10 It is still another aspect of the invention to provide
11 a plurality of structures that can be constructed using
12 such semiconductor dies.

13
14 The invention is directed to methods of fabricating
15 semiconductor die with micro-pins and several
16 embodiments of the structure. The micro-pins
17 fabricated on the semiconductor die can be utilised to
18 stack ICs on top of each other or vertically, or
19 horizontally adjacent to each other. The micro-pins
20 can be used to establish temporary chip attachment
21 points for testing purposes. The micro-pins can also
22 be used to assemble heterogeneous systems; for example,
23 involving attachment of a photo diode on a silicon
24 chip.

25
26 Thus, one aspect of the invention is directed to a
27 semiconductor die comprising a planar semiconductor
28 member; and a plurality of conductive pins extending
29 from the semiconductor member in a direction parallel
30 to a plane of the semiconductor member. The pins may
31 extend directly from the semiconductor member. The

1 semiconductor die may have a plurality of sides, with
2 the pins extending from at least one of the sides or
3 all of the sides, generally in a direction
4 perpendicular to a plane of the semiconductor member.

5
6 The semiconductor die may be combined with at least one
7 additional semiconductor die, the semiconductor dies
8 being disposed one over another so that respective pins
9 of the semiconductor die are stacked one over to
10 facilitate electrical contact with one another. The
11 respective pins may be diffusion bonded to one another
12 to provide the electrical contact or an electrically
13 conductive material may be disposed between the
14 respective pins so as to provide the electrical
15 contact. The combination may further comprise a
16 substrate on which the combination is mounted. The
17 substrate may be formed of a semiconductor material. A
18 second substrate, on which the first substrate may be
19 mounted, may be formed of an insulating material.

20
21 The semiconductor die in accordance with the invention
22 may be combined with at least one other semiconductor
23 die so that successive ones of the semiconductor dies
24 are assembled with at least one wiring substrate
25 between dies, so as to form a solid rectangle or cube.
26 The at least one wiring substrate may provide
27 electrical connections between the dies.

28
29 At least one additional semiconductor die may be
30 assembled to the outside of the solid rectangle, the

1 additional semiconductor die having electrical
2 connections to at least one of the dies in the solid
3 rectangle. The wiring substrates may have opening
4 therein to facilitate management of heat.

5
6 The invention is also directed to a semiconductor die
7 comprising a planar semiconductor member; with a
8 plurality of first electrically conductive pins formed
9 on a surface of the semiconductor member, the pins
10 having portions extending along a side of the
11 semiconductor member. This semiconductor member may be
12 combined with a second semiconductor member having
13 second electrically conductive pins formed on a surface
14 of the second semiconductor member, the second pins
15 having portions extending along a side of the second
16 semiconductor member, at least a portion of the first
17 pins and the second pins being disposed on the
18 semiconductor members so as to align with one another
19 when the semiconductor members are placed in close
20 proximity to one another, so that electrical contact
21 between respective ones of the first pins and the
22 second pins is facilitated. This combination may
23 further comprise at least one additional semiconductor
24 member, the additional semiconductor member having
25 additional pins, the additional pins having portions
26 extending along a side of the additional semiconductor
27 member, the additional pins being disposed on the
28 additional semiconductor member so as to align with
29 additional pins on an additional side of the first
30 semiconductor member or the second semiconductor member

1 when the additional semiconductor member is placed in
2 close proximity to the first semiconductor member or
3 the second semiconductor, so that electrical contact
4 between respective ones of the additional pins and the
5 first pins or second pins is facilitated. The
6 semiconductor members are disposed so as to be
7 coplanar.

8
9 The invention is further directed to a semiconductor
10 die substrate comprising a planar semiconductor member,
11 the member having a plurality of micro-cups formed on a
12 surface thereof, at least a portion of the micro-cups
13 being sized, shaped and positioned so as to receive
14 micro-pins. The semiconductor die may be combined with
15 a second semiconductor die. The second semiconductor
16 die may comprise a planar semiconductor member; a
17 plurality of conductive micro-pins extending from the
18 semiconductor member in a direction parallel to a plane
19 of the semiconductor member, with the micro-pins being
20 received in the micro-cups. Preferably, the
21 semiconductor die substrate and the second
22 semiconductor die are perpendicular to one another.
23 The combination may further comprise at least one
24 bracket member, the bracket member having a first
25 surface in contact with the semiconductor die substrate
26 and a second surface in contact with the second
27 semiconductor die.

28
29 The combination may also further comprise an adhesive
30 material disposed between the semiconductor members to

1 facilitate the semiconductor members being secured to
2 one another.

3
4 The invention is also directed to a method for forming
5 a semiconductor die, comprising forming a trench in a
6 surface of the die; filing the trench with a
7 sacrificial material; patterning the die to form a
8 series of channels extending substantially
9 perpendicularly to the trench; depositing a conductive
10 material in the channels; removing at least a portion
11 of the sacrificial material; and removing portions of
12 the die under the trench so as to separate a portion of
13 the die on one side of the trench from a portion on
14 another side of the trench. The method may further
15 comprise patterning the sacrificial material so that
16 the channels extend so as to be partially in a portion
17 of the die and partially a portion of the sacrificial
18 material. The sacrificial material may be patterned to
19 a depth greater than the die. The removing may be
20 performed by grinding or etching of the die.

21
22 The die may be part of a wafer having a plurality of
23 dies, and the trench may be a dicing lane of the wafer.
24 The sacrificial material may be a polymer or a
25 photoresist. The conductive material may be one of a
26 metal, a conductive paste, and a solder.

27
28 The method may further comprise depositing an adhesion
29 layer in the channels prior to depositing the

1 conductive material. The adhesion layer may be formed
2 of a polymer or a silicon oxide.

3
4 The invention is further directed to a method for
5 forming a semiconductor die, comprising forming a
6 trench in a surface of the die; filing the trench with
7 a sacrificial material; patterning the die to form a
8 series of channels extending substantially
9 perpendicularly to the trench; depositing a conductive
10 material in the channels; removing portions of the die
11 under the trench; and removing at least a portion of
12 the sacrificial material so as to separate a portion of
13 the die on one side of the trench from a portion on
14 another side of the trench.

15
16 In accordance with one additional aspect, the invention
17 is also directed to a method of forming substrates with
18 at least one micro-cup, comprising forming at least one
19 via in the substrate; coating the at least one via with
20 a conductive material or a conductive and adhesive
21 material to form the micro-cup; and coating adhesive
22 material on the substrate to facilitate attachment of a
23 device having at least one pin, the at least one pin
24 being sized, shaped and positioned to be received in a
25 respective one of the at least one via. The method may
26 further comprise assembling the device to the
27 substrate.

28
29
30

1 BRIEF DESCRIPTION OF THE DRAWINGS

2
3 These and other aspects, features, and advantages of
4 the present invention will become apparent upon further
5 consideration of the following detailed description of
6 the invention when read in conjunction with the drawing
7 figures, in which:

8
9 FIG. 1 is a plan view of an embodiment of a
10 semiconductor die with micro-pins of the present
11 invention.

12
13 FIGS. 2A-2Q are cross sectional side views showing
14 process steps to fabricate a semiconductor die with
15 micro-pins as well as the forming of electrical
16 connection between micro-pins and devices on the
17 semiconductor die, while Fig. 2B(i) is a plan view of a
18 portion of Fig 2A.

19
20 FIGS. 3A-3F are side views of an alternate embodiment
21 showing stacking of semiconductor chips using
22 micro-pins in accordance with the present invention.

23
24 FIGS. 4A-4C are side views of an alternate embodiment
25 showing attachment of semiconductor die stack on
26 another semiconductor die, interposer, or a substrate.

27
28 FIGS. 5A-5B are side views of an alternate embodiment
29 of the invention showing attachment of semiconductor
30 die stack on a substrate.

1
2 FIGS. 6A-6B are frontal and edge view of a
3 semiconductor die with micro-pins.

4
5 FIG. 7A-7B are side views of an alternate embodiment
6 showing semiconductor chips with micro-pins assembled
7 vertically adjacent to each other on a substrate.

8
9 FIG. 8A-8B is an alternate embodiment showing
10 semiconductor chips with micro-pins assembled in a cube
11 surrounding by multiple substrates.

12
13 FIG. 9 is a side elevational view of semiconductor chip
14 cube of Fig 8A.

15
16 FIG. 10A-10D are sectional views showing process steps
17 to fabricate micro-cups on a substrate.

18
19 FIG. 11A is a plan view and FIG. 11B is a cross
20 sectional view which illustrate an alternate embodiment
21 showing vertical or horizontal attachment of devices,
22 such as Group III-V devices, on a silicon chip using
23 micro-pins and micro-cups.

24
25 Fig. 12 is a plan view of horizontal tiling of
26 semiconductor dies in accordance with yet another
27 aspect of the invention.

1 DESCRIPTION OF THE INVENTION

2
3 Variations described for the present invention can
4 be realized in any combination desirable for each
5 particular application. Thus particular limitations,
6 and/or embodiment enhancements described herein,
7 which may have particular advantages to the
8 particular application need not be used for all
9 applications. Also, it should be realized that not all
10 limitations need be implemented in methods, systems
11 and/or apparatus including one or more concepts of the
12 present invention.

13
14 Referring to the drawings more particularly by
15 reference numbers, Fig. 1 shows an embodiment of a
16 semiconductor die 20 with micro-pins 22 of the present
17 invention. The semiconductor die may include plurality
18 of micro-pins on any one or all sides of the die.
19 These micro-pins are electrically connected to devices
20 on the die 20. Typical dimensions for the micro-pins
21 22 may be a length of 1 to 1000 microns, a width of 1
22 to 500 microns and a depth of 1 to 800 microns in the
23 direction into the die 20, although these dimensions
24 are provided merely by way of example. Actual
25 dimensions will depend on the requirements of the
26 specific application.

27
28 Fig. 2A and Fig. 2B show first steps in the process of
29 fabricating semiconductor die with micro-pins 22. A
30 portion 24 of a typical semiconductor wafer having

1 chips 20 separated by dicing lanes or kerfs 26,
2 extending in two mutually perpendicular directions so
3 as to form rectangular dies, is shown in Fig. 2A. The
4 widths of these dicing lanes or kerfs 26 is application
5 dependent.

6
7 As shown in Fig. 2B and Fig. 2B(i), trenches 28 may be
8 created on the wafer with known wet or dry etching
9 processes. The trenches 28, having dimensions which
10 may vary with the application, may be placed at least
11 partially in the dicing lanes or kerfs 26, and have
12 extensions 30 which are used to form the micro-pins 22.
13 The trenches 28 and their extensions 30 may be filled
14 with a sacrificial epoxy, polymer, photoresist or
15 similar material 31 as shown in FIG. 2C.

16
17 Using known photolithographic process, the polymer or
18 polymer like material may be patterned and etched using
19 wet or dry etching processes as shown in FIG. 2D(i) and
20 2D(ii). The wet or dry etching processes may be
21 selective with respect to semiconductor material and
22 may allow the formation of a specific structure, such
23 as, for example, the channel 32 of Fig. 2D(i) or the
24 step structure 34 as shown in FIG. 2D(ii).

25
26 The patterned and etched features may be filled with
27 conductive material such as copper, metallic paste,
28 solder, etc. to form micro-pins 22 as shown in FIG.
29 2E(i), for the case of the pattern formed in Fig.
30 2D(i), and the micro-pins 22A of Fig. 2E(ii), for the

1 case of the pattern formed in Fig. 2D(ii). Prior to
2 filling the patterned features with conductive
3 material, layers of passivation films such as silicon
4 oxide or silicon nitride, adhesive films such as
5 polymeric or epoxy materials or metals such as indium,
6 tin, and plating seed or barrier layers such as
7 titanium, tantalum, chromium or copper may be deposited
8 in the patterned features.

9
10 As an optional step, additional conductive materials 36
11 such as metals or conductive polymers may be patterned,
12 coated or deposited on top of micro-pins as shown in
13 FIG. 2F(i) and FIG. 2F(ii). The polymer like material
14 31 deposited in the trenches as described above with
15 respect to FIG. 2C may be removed partially or
16 completely from the trenches as shown in FIG. 2G(i) and
17 Fig. 2G(ii).

18
19 Using a laser saw or dicing saw or any other known
20 method, the semiconductor wafer may be diced from the
21 back side as shown in FIG. 2H(i) and Fig 2H(ii). Waste
22 portions 40 are discarded. As part of the
23 dicing/singulating process, the wafer may temporarily
24 be attached to a dicing tape or substrate (not shown).
25 The process sequence described in FIG. 2a-2h results
26 into individual semiconductor dies with micro-pins 22
27 or 22A. Micro-pins 22 are essentially embedded in the
28 surface of die 20. Micro-pins 22 then extend in a
29 cantilevered fashion horizontally away from die 20.
30 Micro-pins 22A also may be embedded in the surface of

1 die 20. However, micro-pins 22A have a portion 23
2 extending downward and against the vertical side
3 surface of die 20.
4

5 An alternate process of fabricating semiconductor die
6 with micro-pins is described in FIGS. 2I-2K.
7 Preferably, immediately following process step
8 described in FIG. 2F(i) or FIG. 2F(ii), the wafer may
9 be ground from the backside as shown in FIG. 2I(i) and
10 FIG. 2I(ii). During the backside grind step, the front
11 side of the semiconductor wafer temporarily may be
12 attached to an adhesive tape or a substrate (not
13 shown). The backside grind step may include a coarse
14 grind, a fine grind and a chemical mechanical polishing
15 (CMP) steps. The backside grinding of the
16 semiconductor wafer may stop when the polymer like film
17 or conductive material is exposed as shown in FIG.
18 2I(i) and FIG. 2I(ii).
19

20 The semiconductor material on the backside of the wafer
21 may be removed or etched using wet or dry processes as
22 shown in FIG. 2J(i) or Fig 2J(ii). The polymer like
23 material deposited in the trenches as described above
24 with respect to FIG. 2C may be removed as shown in FIG.
25 2K(i) and FIG. 2K(ii). The process sequence described
26 in FIG. 2I-2K results in individual semiconductor dies
27 with micro-pins 22B or 22C, which extend below the back
28 side of the respective dies 20. Referring to Fig.
29 2K(i) specifically, micro-pins 22B are formed with a
30 lower portion 25 that extends below die 20. Referring

1 to Fig. 2K(ii) specifically, micro-pins 22C extend
2 downward and against the vertical side surface of die
3 20 and below die 20. Micro-pins 22B and 22C are
4 especially advantageous in allowing dies having
5 micro-pins with these configuration to be stacked, as
6 described in more detail below.

7
8 The semiconductor dies with micro-pins produced using
9 the process of FIG. 2I to FIG. 2K can be very thin (1
10 to 400 micrometers thick) and the requirement of dicing
11 the wafer to obtain individual dies is avoided.
12 Although not specifically mentioned above, the step
13 involving removal of polymer like material, as
14 described with respect to FIG. 2K, may be exercised
15 prior to the step of grinding the wafer from the back
16 as described with respect to FIG. 2I.

17
18 FIG. 2L Fig. 2Q illustrate steps in forming an
19 electrical connection between the micro-pins and
20 devices on the semiconductor die. A sectional view of
21 a semiconductor die on a semiconductor wafer at the end
22 of final passivation step, having a final passivation
23 layer 42 is shown in FIG. 2L. At this point, die
24 terminal pads 44 are covered with the final passivation
25 layer 42. Micro-pin fabrication process steps described
26 in FIG. 2B to FIG. 2C may be applied to the
27 semiconductor wafer 20 as shown in FIG. 2M, to produce,
28 for example, micro-pins 22A.

29

1 Using known photolithographic process, a photo-
2 polymeric material 31 may be patterned onto the wafer
3 in FIG. 2N. As part of process step illustrated in
4 FIG. 2D, the photo-polymer material 31 may be patterned
5 such that it uncovers the trench and die terminal pads
6 44 which are covered in FIG. 2N. The polymer like
7 material 31 in the trench and the passivation material
8 42 on top of die terminal pads 44 may be partially
9 etched (partially uncovering a terminal pad 44A) or
10 completely etched (completely uncovering a terminal pad
11 44B) using wet or dry processes as shown in FIG. 2O, in
12 the manner described with respect to FIG. 2D(i) and
13 FIG. 2D(ii).

14

15 Referring to FIG. 2P, the patterned and etched
16 features may be filled with conductive material 48 such
17 as copper, metallic paste, solder, etc to form
18 micro-pins 22C. Prior to filling the patterned
19 features with conductive material, layers of
20 passivation films such as silicon oxide or silicon
21 nitride, adhesive films such as polymeric or epoxy
22 materials or metals such as indium, tin, and plating
23 seed or barrier layers such as titanium, tantalum,
24 chromium and copper may be deposited in the patterned
25 features.

26

27 Referring to Fig. 2Q, the photo-polymer material 46 may
28 be removed from the wafer surface to produce the
29 structure shown therein. The process steps described
30 with respect to FIGS. 2L to FIG. 2Q may be performed.

1 Electrical connections 50A and 50B may then be made to
2 the micro-pins 22A and to devices (not shown) on the
3 die 20 by means of die terminal pads 44A and 44B. The
4 wafer may be subjected to process steps described with
5 respect to FIG. 2F to FIG. 2h or FIG. 2I to FIG. 2K to
6 obtain a semiconductor die with micro-pins.

7
8 FIG. 3A to FIG. 3F are side views of various
9 embodiments showing stacking of semiconductor chips
10 using micro-pins and/or joining material formed on top
11 of micro-pins. In FIG. 3A the dies 20 have micro-pins
12 22B. In FIG. 3B the dies 20 have micro-pins 22A, which
13 extend below the lower surface or back side of dies 20.
14 The application of suitable heat and pressure may
15 result in diffusion bonding of the micro-pins. The
16 embodiment of FIG. 3C is similar to that of FIG. 3A,
17 but a joining material 54 is used between the
18 micro-pins 22B of successive dies 20. In FIG. 3D, a
19 joining material 54 is used between the micro-pins 22C
20 of successive dies 20. In FIG. 3E, a chip formed on a
21 relatively smaller die 20A is stacked on top of a
22 chip formed on a relatively larger die 20B. A joining
23 material 54 is used between the bottom surface of
24 micro-pins 22B and the top surface of die 20B. In FIG.
25 3F, the lower surfaces of micro-pins 22C of a die 20A
26 may be placed on the upper surface of a die 20B, with
27 or without the use of a joining layer. If no joining
28 layer is used, diffusion bonding may be utilised.
29 These embodiments may be employed when stacking of thin
30 semiconductor chips of same or different sizes on top

1 of each other is desired to gain electrical performance
2 or to achieve a compact, dense system that fully
3 utilises three-dimensional integration.

4
5 FIG. 4A to FIG. 4C are side elevational views of
6 alternate embodiments showing attachment of a
7 semiconductor dies stack 60 on another semiconductor
8 die, on an interposer, or on a substrate. As shown in
9 FIG. 4A, the semiconductor die stack 60, comprising
10 memory chips, for example, may be attached to a
11 semiconductor die, a substrate or an interposer 61 to
12 construct a complex, high performance multi-chip module
13 shown generally as 62. Substrate 61 may itself have
14 micro-pins of the type 22A to which stack 60 is
15 attached. Attachment may be effected using attachment
16 members 63 such as a solder ball, conductive adhesive,
17 or a metal, as is well known in the art. Attachment
18 members 63A may be used to affix and electrically
19 connect multi-chip module 62 to the next level of
20 packaging.

21
22 FIG. 4B is a side elevational view of stacking of the
23 chip module 62 of FIG. 4A onto another semiconductor
24 interposer 68. Similarly, as shown in FIG. 4C, chip
25 modules 62 of kind illustrated in FIG. 4A may be
26 stacked on top of each other, by interposing a spacer
27 70 to achieve an extremely dense high performance
28 system, shown generally as 72.

29

1 FIG. 5A and FIG. 5B are side elevational views of
2 alternate embodiments showing attachment of a
3 semiconductor die stack 60 to a non-semiconductor
4 substrate 80 of a next level of packaging such as a
5 ceramic substrate, FR-4 board or a high density
6 substrate. In FIG. 5A, the stack 60 of dies is
7 connected directly to the non-semiconductor substrate
8 80 by means of a metal, solder or conductive adhesive,
9 which may be in the form of attachment members 82. An
10 underfill material 83, such as an epoxy or polymer
11 resin may then be applied. In FIG. 5B, a chip module
12 shown generally as 65 is connected directly to a
13 substrate 84 by means of a metal, solder conductive
14 adhesive, which may be in the form of attachment
15 members 86. Substrate 84 is then connected to a
16 substrate 80 by means of a metal, solder, or conductive
17 adhesive, which may be in the form of attachment
18 members 88. An underfill 83 may also be applied. These
19 embodiments may be used in creating a high performance
20 computer where the substrates shown in FIG. 5A or FIG.
21 5B are then connected in parallel, through a backplane
22 (not shown), to a cabinet panel (also not shown).

23

24 FIG. 6A and FIG. 6B are plan and perspective views,
25 respectively, of a semiconductor die 20 with micro-pins
26 22 on one of its sides.

27

28 FIG. 7A and Fig 7B are perspective views of an
29 alternate embodiment showing semiconductor chips or
30 dies 20 with micro-pins 22 assembled vertically

1 adjacent to each other on a substrate. The
2 semiconductor dies, each with micro-pins on one of its
3 sides, may be attached to a substrate vertically
4 adjacent to each other as shown in FIG. 7A. This
5 embodiment is useful when it is desired to achieve a
6 high packing density or to provide a highly compact
7 system, by assembling chips adjacent to each other
8 rather, than on top of each other. Assembling chips
9 adjacent to each other is especially attractive when
10 the chips have differing dimensions. In contrast to
11 attaching a die so that it is flat on the substrate,
12 vertical attachment of semiconductor dies using
13 micro-pins as described by this embodiment also assists
14 in reducing thermo-mechanical stresses arising as a
15 result of difference in the Coefficient of Thermal
16 Expansion (CTE) that typically exists between a
17 semiconductor die and a non-semiconductor substrate
18 such as an FR-4 board or a high density substrate.
19 This is because the distance from die neutral point
20 (DNP) on the substrate is significantly reduced in
21 vertical assembly, as opposed to that in horizontal
22 assembly. Vertically assembled chips as shown in FIG.
23 7A may be firmly supported by specially designed
24 mechanical clamps or fixtures 92 as shown in FIG. 7B.

25
26 FIG. 8A is an alternate embodiment showing
27 semiconductor chips or dies 20 with micro-pins 22
28 assembled in a rectangular solid or a cube and attached
29 to wiring backplanes, substrates or interposers 96, and
30 in the form of a cube 100. This is a useful embodiment

1 when an extremely dense system is desired. For
2 example, memory chips can be assembled in a cube
3 surrounding by wiring planes and respective processor
4 or logic chips 102 can be assembled on the wiring
5 substrate as shown in FIG. 8B. As such, processor or
6 logic chips can readily access memory that is assembled
7 in the cube. The semiconductor chips or dies 29 with
8 micro-pins 22 can be assembled to form a rectangular
9 solid or more particularly the cube 100 by joining the
10 chips to the wiring backplanes, substrates or
11 interposers 96 having dual or single sided wiring and a
12 surface metallurgy that is able to bond by means of
13 metal, solder or electrically conductive adhesive. In
14 this case, the wiring backplanes or substrates will
15 form the faces of the cube 100 with singular or
16 multiple chips inside such cube. Once such system is
17 constructed, the additional chips 102 can be readily
18 attached to the outer side of the wiring backplanes or
19 substrates forming the cube by similar means of metal,
20 solder or electrically conductive adhesive.

21

22 FIG. 9 shows a side elevational view of the cube system
23 shown in FIG. 8. The wiring plane or substrates 96 of
24 the cube system may have holes/slots 104 in them to
25 allow for thermal management, as for example, by
26 circulating a cooling fluid through the holes or slots
27 104. The wiring planes 96A at opposite sides of the
28 cube 100 may additionally have connectors 106 that
29 allow attachment of the system to the next higher level
30 of packaging.

1 FIG. 10A to FIG. 10D are sectional views showing
2 process steps to fabricate micro-cups on a substrate
3 that may be useful in making electrical and mechanical
4 connection between semiconductor dies with micro-pins
5 and the substrate, as well as to other components on
6 the substrate. Via cups 108 may be formed, by any
7 known wet or dry chemical process, in the substrate 110
8 as shown in FIG. 10A. The substrate may be a
9 semiconductor die, package interposer, or of other
10 forms as used in the electronics industry. Vias for
11 this purpose may also vary in size and shape. The vias
12 may be filled or coated with adhesive and/or conductive
13 material 112 as shown in FIG. 10B. Such adhesive or
14 conductive material may help in achieving an electrical
15 and mechanical connection between the device with
16 micro-pins and the substrate. Micro-pins may be
17 connected to other points on the substrate by use of
18 electrical connections that are made to micro-cups, by
19 for example, a thin electrically conductive layer 114,
20 deposited on the surface of substrate 110, which
21 extends into cups 108, as shown in FIG. 10C(i) and FIG.
22 10C(ii). Additionally, a layer of adhesive material
23 116 may be coated on the substrate to act as "glue"
24 between the semiconductor die with micro-pins and the
25 substrate 110. Layer 116 may be one of a polymer, an
26 epoxy, or a silicon dioxide layer which forms a bond
27 under suitable temperature and pressure conditions. A
28 device 118 having micro-pins 122 is assembled to a
29 substrate 110, as shown in Fig. 10D.

30

1 FIG. 11A and FIG. 11B illustrate an alternate
2 embodiment showing vertical or horizontal attachment of
3 devices, such as a Group III-V (compound semiconductor,
4 such as GaAs, InP) device or other device 124, on a
5 silicon chip or die 140. The die 140 has micro-pins
6 142, while the device 124 has micro-pins 144, which
7 are received in micro-cups 148. This embodiment is
8 useful when it is necessary to build heterogeneous
9 system. The device 124 is attached at a point in the
10 fabrication process later than that at which micro-pins
11 143 are formed.

12
13 Fig. 12 illustrates an embodiment of the invention
14 wherein dies 20 having micro-pins 22 are arranged in a
15 horizontal plane so that the ends of micro-pins of one
16 die are in physical contact with the ends of micro-pins
17 22 of an adjacent die. Although the ends are shown as
18 being in contact, in principle, the dies may be
19 positioned so that the sides of the micro-pins 22 of
20 one die contact the sides of the micro-pins 22 of an
21 adjacent die. In either case, electrical connection
22 between the micro-pins 22 may be made with a solder, a
23 conductive adhesive, or by diffusion bonding of the
24 micro-pins of one die to the micro-pins of an adjacent
25 die under suitable temperature and pressure conditions.
26 This "tiling" arrangement is especially advantageous in
27 that it provides an extremely high bandwidth connection
28 between the dies.

29

1 The present invention advantageously has advantages and
2 other uses not specifically discussed above. For
3 example, micro-pins and micro-cups may provide
4 attachment or connection points for the testing of
5 chips. In such case, micro-pins can temporarily be
6 used to test the chips when fabricated, as well as
7 attachment of chips to next level of packaging, after
8 testing.

9
10 While certain exemplary embodiments have been described
11 and shown in the accompanying drawings, it is to be
12 understood that such embodiments are merely
13 illustrative of and not restrictive on the broad
14 invention, and that this invention not be limited to
15 the specific constructions and arrangements shown and
16 described, since various other modifications may occur
17 to those ordinarily skilled in the art.

18
19 It is noted that the foregoing has outlined some of the
20 more pertinent objects and embodiments of the present
21 invention. The concepts of this invention may be used
22 for many applications. Thus, although the description
23 is made for particular arrangements and methods, the
24 intent and concept of the invention is suitable and
25 applicable to other arrangements and applications. It
26 will be clear to those skilled in the art that other
27 modifications to the disclosed embodiments can be
28 effected without departing from the spirit and scope of
29 the invention. The described embodiments ought to be
30 construed to be merely illustrative of some of the more

1 prominent features and applications of the invention.
2 Other beneficial results can be realized by applying
3 the disclosed invention in a different manner or
4 modifying the invention in ways known to those familiar
5 with the art. Thus, it should be understood that the
6 embodiments has been provided as an example and not as
7 a limitation. The scope of the invention is defined by
8 the appended claims.
9